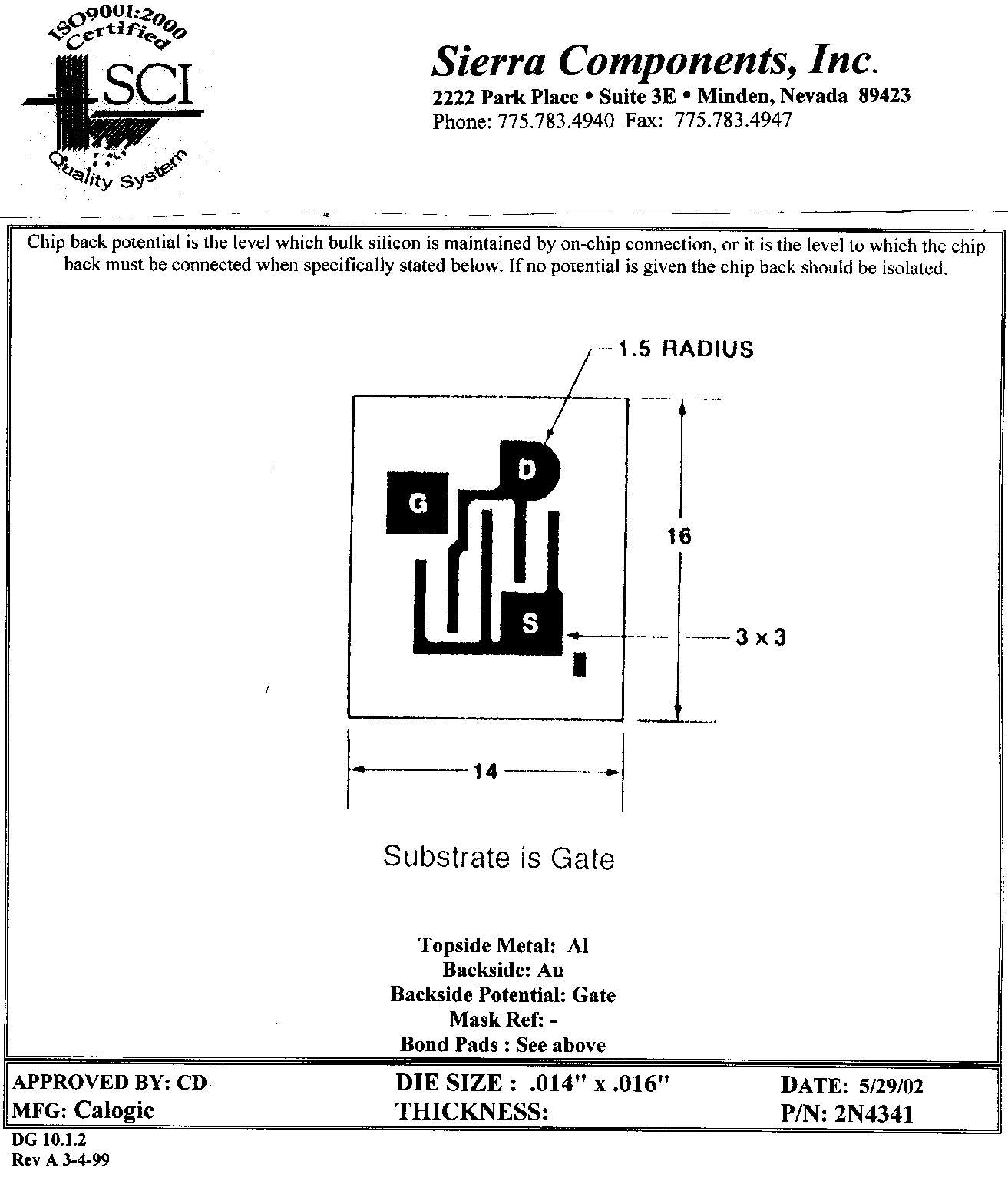
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.014”**

**.016”**

**RADIUS .015”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size = .003 x .003”**

**Substrate = GATE**

**Mask Ref: 5010**

**APPROVED BY: DK DIE SIZE .014” X .016” DATE: 8/25/21**

**MFG: CALOGIC THICKNESS .008” P/N: SST204-210**

**DG 10.1.2**

#### Rev B, 7/1